AMENDMENTS TO THE CLAIMS

1. (Original) A pulse width modulation (PWM) buffer circuit comprising:

a duty cycle converting circuit for receiving a first PWM signal and then generating a duty cycle reference voltage based on a first duty cycle of the first PWM signal, wherein the duty cycle reference voltage is a one-to-one mapping function of the first duty cycle, and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting a second PWM signal having a fixed frequency, wherein the second PWM signal has a second duty cycle determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage.

2. (Original) The PWM buffer circuit according to claim 1, wherein the duty cycle converting circuit comprises:

a transistor having a gate for receiving the first PWM signal and a source coupled to ground;

a first resistor connected between a drain of the transistor and a voltage source;

a diode having a P electrode connected to the drain of the transistor;

a second resistor connected between an N electrode of the diode and the ground;

a first capacitor connected between the N electrode of the diode and the ground;

a first operational amplifier having a non-inverting input terminal connected to the N electrode of the diode;

a third resistor connected between an inverting input terminal of the first operational amplifier and the ground;

a fourth resistor connected between the inverting input terminal of the first operational amplifier and an output terminal of the first operational amplifier; and

a fifth resistor connected between the output terminal of the first operational amplifier and the frequency-fixed PWM signal generating circuit.

3. (Original) The PWM buffer circuit according to claim 1, wherein the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs.

4. (Original) The PWM buffer circuit according to claim 1, wherein the frequency-fixed PWM signal generating circuit comprises:

a frequency controller for providing a frequency control signal to determine the fixed frequency of the second PWM signal, and

a PWM signal generator, coupled to the duty cycle converting circuit and the frequency controller, for generating the second PWM signal in response to the duty cycle reference voltage and the frequency control signal.

5. (Currently Amended) The PWM buffer circuit according to claim 4, wherein the frequency controller comprises:

an ~~second operational~~operational amplifier having a non-inverting input terminal, an inverting input terminal, and an output terminal;

a ~~sixth resistor~~first resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the ground;

a ~~seventh resistor~~second resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the output terminal of the ~~second operational~~operational amplifier;

a ~~second capacitor~~capacitor connected between the inverting input terminal of the ~~second operational~~operational amplifier and the ground; and

~~an eighth resistor~~third resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the output terminal of the ~~second operational~~operational amplifier.

6. (Currently Amended) The PWM buffer circuit according to claim 4, wherein the PWM signal generator comprises:

an ~~third operational~~operational amplifier having a non-inverting input terminal connected to the duty cycle converting circuit for receiving the duty cycle reference voltage and an inverting terminal connected to the frequency controller for receiving the frequency control signal, and

a ~~ninth resistor~~resistor having a terminal connected to an output terminal of the ~~third operational~~operational amplifier such that the second PWM signal is output through another terminal of the ~~ninth resistor~~resistor.

7. (Original) The PWM buffer circuit according to claim 4, wherein the frequency control signal is a continuous triangular wave signal.

8. (Currently Amended) The PWM buffer circuit according to claim 1, wherein a frequency of the first PWM signal is higher

than 30 Hz and the first duty cycle ~~is located between~~ ranges from5% and 95%.

9. (Original) The PWM buffer circuit according to claim 1, wherein the fixed frequency of the second PWM signal is higher than 10 kHz.

10. (Original) A control circuit for speed of a fan motor, comprising:

a PWM signal generation unit for generating a first PWM signal having a first duty cycle;

a PWM buffer circuit, coupled to the PWM signal generation unit, for converting the first PWM signal into a second PWM signal having a fixed frequency and a second duty cycle; and

a driving circuit, coupled to the PWM buffer circuit, for outputting a driving signal based on the second PWM signal to the fan motor, thereby controlling the speed of the fan motor.

11. (Original) The control circuit according to claim 10, wherein the PWM buffer circuit comprises:

a duty cycle converting circuit for receiving the first PWM signal and then generating a duty cycle reference voltage based on the first duty cycle of the first PWM signal, wherein the duty

cycle reference voltage is a one-to-one mapping function of the first duty cycle, and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting the second PWM signal, wherein the second duty cycle of the second PWM signal is determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage.

12. (Original) The control circuit according to claim 10, wherein the duty cycle converting circuit comprises:

a transistor having a gate for receiving the first PWM signal and a source coupled to ground;

a first resistor connected between a drain of the transistor and a voltage source;

a diode having a P electrode connected to the drain of the transistor;

a second resistor connected between an N electrode of the diode and the ground;

a first capacitor connected between the N electrode of the diode and the ground;

a first operational amplifier having a non-inverting input terminal connected to the N electrode of the diode;

a third resistor connected between an inverting input terminal of the first operational amplifier and the ground;

a fourth resistor connected between the inverting input terminal of the first operational amplifier and an output terminal of the first operational amplifier; and

a fifth resistor connected between the output terminal of the first operational amplifier and the frequency-fixed PWM signal generating circuit.

13. (Original) The control circuit according to claim 10, wherein the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs.

14. (Original) The control circuit according to claim 10, wherein the frequency-fixed PWM signal generating circuit comprises:

a frequency controller for providing a frequency control signal to determine the fixed frequency of the second PWM signal, and

a PWM signal generator, coupled to the duty cycle converting circuit and the frequency controller, for generating the second PWM signal in response to the duty cycle reference voltage and the frequency control signal.

15. (Currently Amended) The control circuit according to claim 14, wherein the frequency controller comprises:

a ~~second operational~~operational amplifier having a non-inverting input terminal, an inverting input terminal, and an output terminal;

a ~~sixth resistor~~first resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the ground;

a ~~seventh resistor~~second resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the output terminal of the ~~second operational~~operational amplifier;

a ~~second capacitor~~capacitor connected between the inverting input terminal of the ~~second operational~~operational amplifier and the ground; and

an ~~eighth resistor~~third resistor connected between the non-inverting input terminal of the ~~second operational~~operational amplifier and the output terminal of the ~~second operational~~operational amplifier.

16. (Currently Amended) The control circuit according to claim 14, wherein the PWM signal generator comprises:

an ~~third operational~~operational amplifier having a non-inverting input terminal connected to the duty cycle converting circuit for receiving the duty cycle reference voltage and an inverting terminal connected to the frequency controller for receiving the frequency control signal, and

a ~~ninth resistor~~resistor having a terminal connected to an output terminal of the ~~third operational~~operational amplifier such that the second PWM signal is output through another terminal of the ~~ninth resistor~~resistor.

17. (Original) The control circuit according to claim 14, wherein the frequency control signal is a continuous triangular wave signal.

18. (Currently Amended) The PWM buffer circuit according to claim 1, wherein a frequency of the first PWM signal is higher than 30 Hz and the first duty cycle ~~is located between~~ ranges from 5% and 95%.

19. (Original) The control circuit according to claim 10, wherein the fixed frequency of the second PWM signal is higher than 10 kHz.